AMENDMENTS

Amendments in the Specification:

Please amend the specification as follows:

On page 3 of the specification, please amend the first full paragraph (lines 2-7) as follows:

Referring to Fig. 3a, when a chip enable signal ~~CSB~~ CEB applied externally transits from a high to low level, and then address is decoded, a corresponding wordline WL is enabled. In other words, a potential of the wordline WL transits from a low to high level, thereby selecting the cell. SEN is a sense amplifier enable signal.

On page 4 of the specification, please amend the first full paragraph (lines 2-4) as follows:

Referring to Fig. 3b, when a chip enable signal ~~CSB~~ CEB externally transits from a high to low level, all bitlines are equalized to a low level by an equalization signal.

On page 4 of the specification, please amend the last paragraph that carries over to page 5 of the specification as follows:

As a result, a sense amplifier enable signal SEN is activated after a predetermined time to enable the sense amplifier. Then, when the data is destroyed, the sense amplifier amplifies the data to output a logic value "0". DOUT refers to output data.

On page 16 of the specification, please amend the third full paragraph 4 (lines 8-12) as follows:

The boosting voltage VPP is applied to the wordline WL earlier than the plateline PL (t2), and then the boosting voltage VPP is applied to the plateline PL. As a result, data stored in the unit cell MC is transmitted into the sub-bitline SBL. CEB is a chip enable signal. /WE is a write enable signal and performs a write operation in a low level of tWP. As described above with respect to other figures, MBLC is a main bitline control signal, MBPUC is a main bitline pull-up control signal, and CSN is a column selecting control signal.

On page 18 of the specification, please amend the last paragraph (lines 22-24) as follows:

Fig. 11 is a timing diagram illustrating a read operation of the disclosed nonvolatile ferroelectric memory device according to the present invention. As described above with respect to other figures, CEB is a chip enable signal, /WE is a write enable signal and performs a write operation in a low level of tWP, DOUT refers to output data, MBLC is a main bitline control signal, MBPUC is a main bitline pull-up control signal, and CSN is a column selecting control signal.

On page 23 of the specification, please amend the second full paragraph (lines 16-17) as follows:

Fig. 15 is a timing diagram illustrating an operation of the wordline driver of Fig. 14. DEC10 is a first signal of the first decoder signal. DEC20 is a first signal of the second decoder signal.

On page 26 of the specification, please amend the first full paragraph (lines 5-6) as follows:

Fig. 17 is a timing diagram illustrating an operation of a plateline driver of Fig. 16. DEC10 is a first signal of the first decoder signal. DEC20 is a first signal of the second decoder signal.

On page 32 of the specification, please amend the first full paragraph (lines 4-5) as follows:

Fig. 21 is a cross-sectional diagram illustrating a cross section diagram of the wordline driver of ~~Fi.~~ Fig. 14.

On page 33 of the specification, please amend the first full paragraph (lines 13-17) as follows:

The transmission lines 91, 92 and 93 are formed in the third layer L3. The transmission line 92 is to transmit the gate boosting voltage GVPP. The transmission lines 91 and 93 are to transmit the second decoder signals DEC20 and DEC21, respectively. References n+ show a source and drain of NMOS transistors.

On page 35 of the specification, please amend the third full paragraph (lines 10-12) as follows:

The address transition detecting circuit 54 comprises an address buffer 55 enabled by a clock enable signal CEBEN, an address latch 56, an address transition detector 57 enabled by the clock enable signal CEBEN, and an address decoder 58.

On page 35 of the specification, please amend the fifth full paragraph (lines 16-18) as follows:

The address latch 56 latches an address latch signal ANLAT in response to operation control signals OP and OPB, and then outputs address signals AAN and AANB. The address

transition detector 57 outputs an address transition detecting signal by using address signals AAN and AANB.

On page 36 of the specification, please amend paragraph 4 (lines 10-22) as follows:

The address latch 56 comprises transmission gates TG1 and TG2, and inverters ~~Inv41~~ INV41, INV42, INV43, INV44 and INV55. The transmission gate TG1 selectively transmits the address latch signal ANLAT in response to the operation control signals OP and OPB. The inverters INV41 and INV42 are latch-connected. The transmission gate TG2 selectively outputs an output signal from the inverter INV42 into an input terminal of the inverter INV41 in response to the operation control signals OP and OPB. The inverter INV43 inverts and output signal from the inverter INV41 to output the address signal AAN. The inverter INV44 and INV45 sequentially inverts the output signal from the inverter INV41, and then to output an inverted address signal AANB.

Amendments to the Drawings:

Applicants submit herewith in Appendix A replacement drawing sheets for Figures 1-3b, 12-17 and 21. Applicants submit corresponding marked-up drawings in Appendix B.